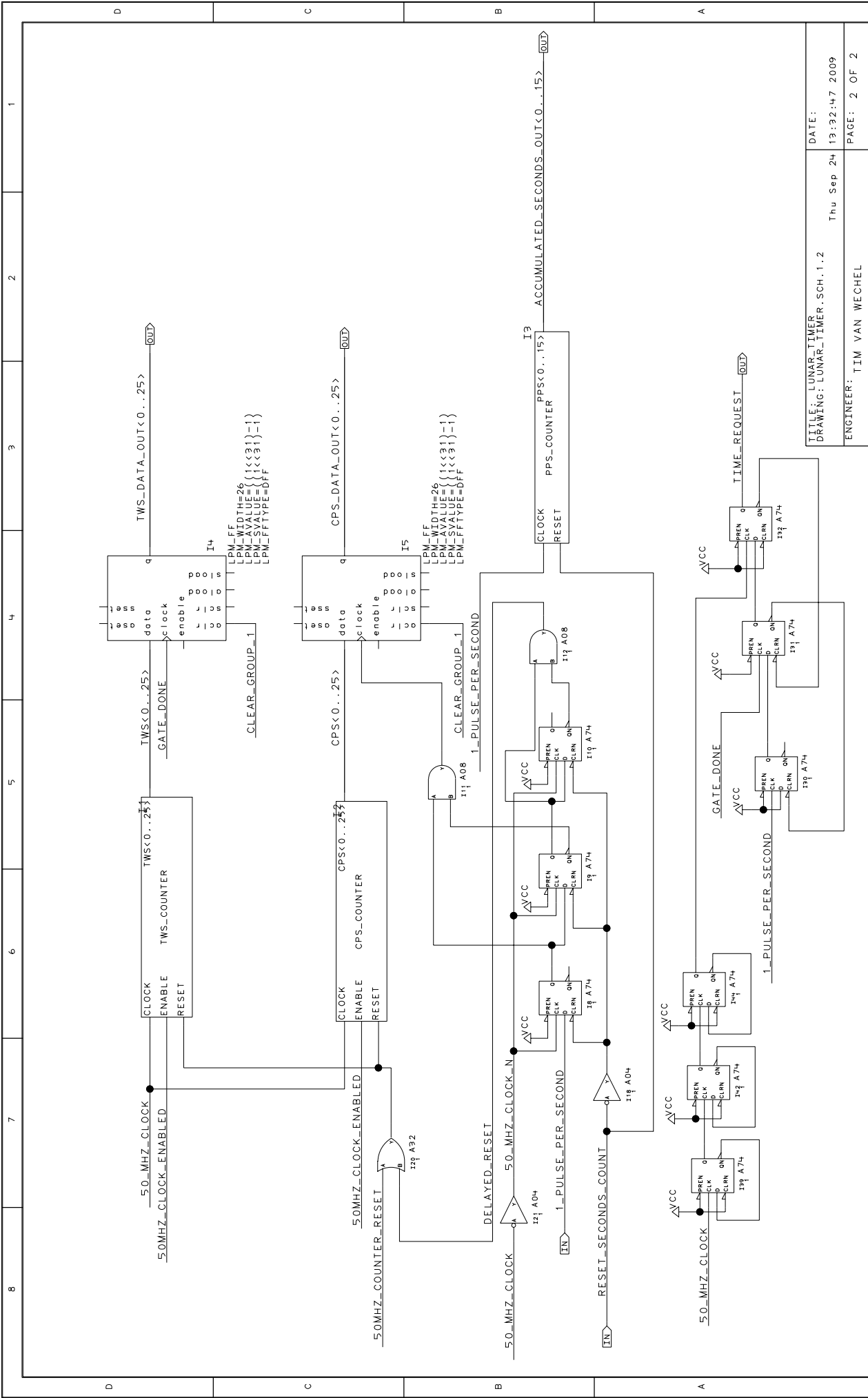
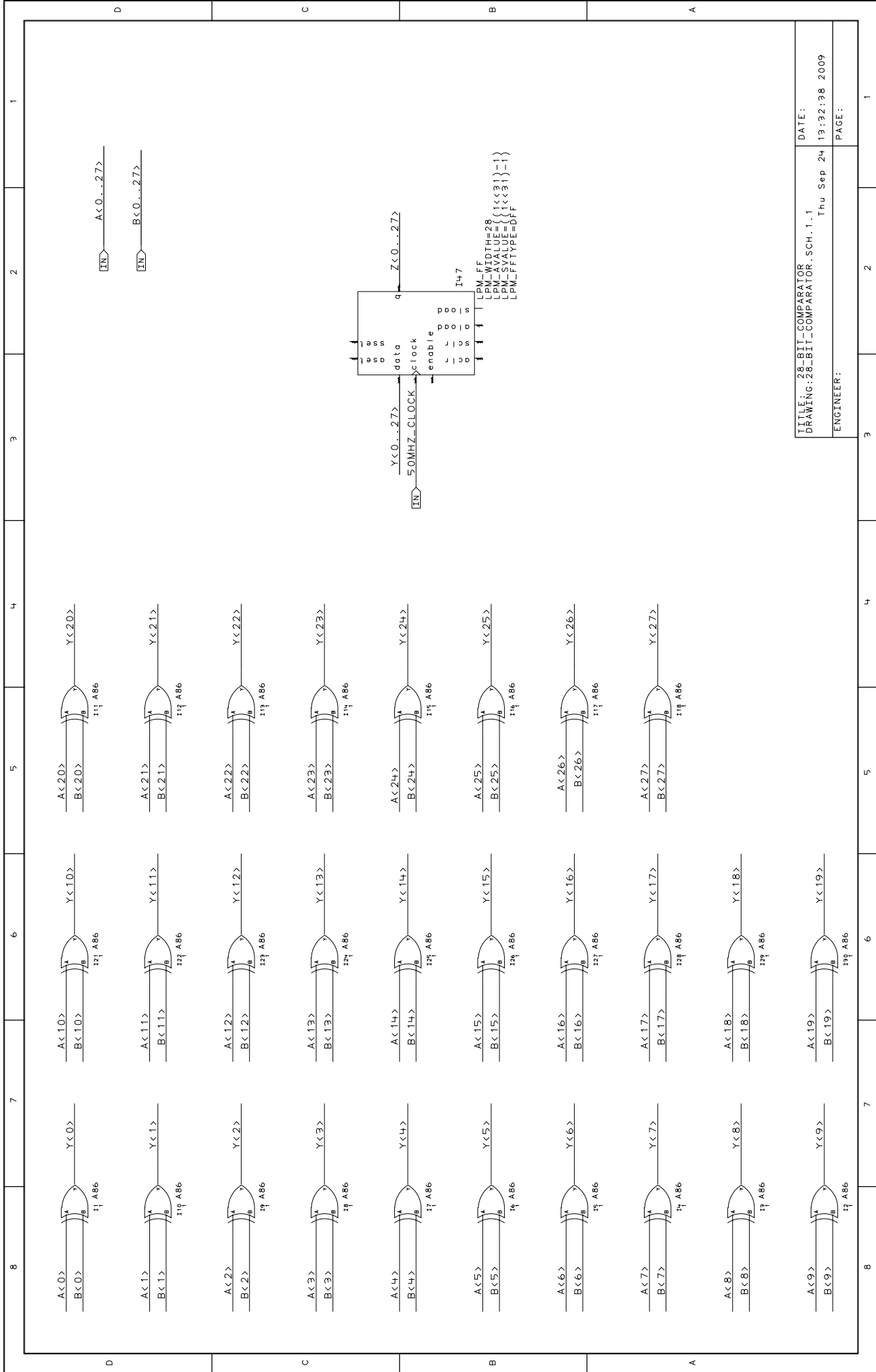


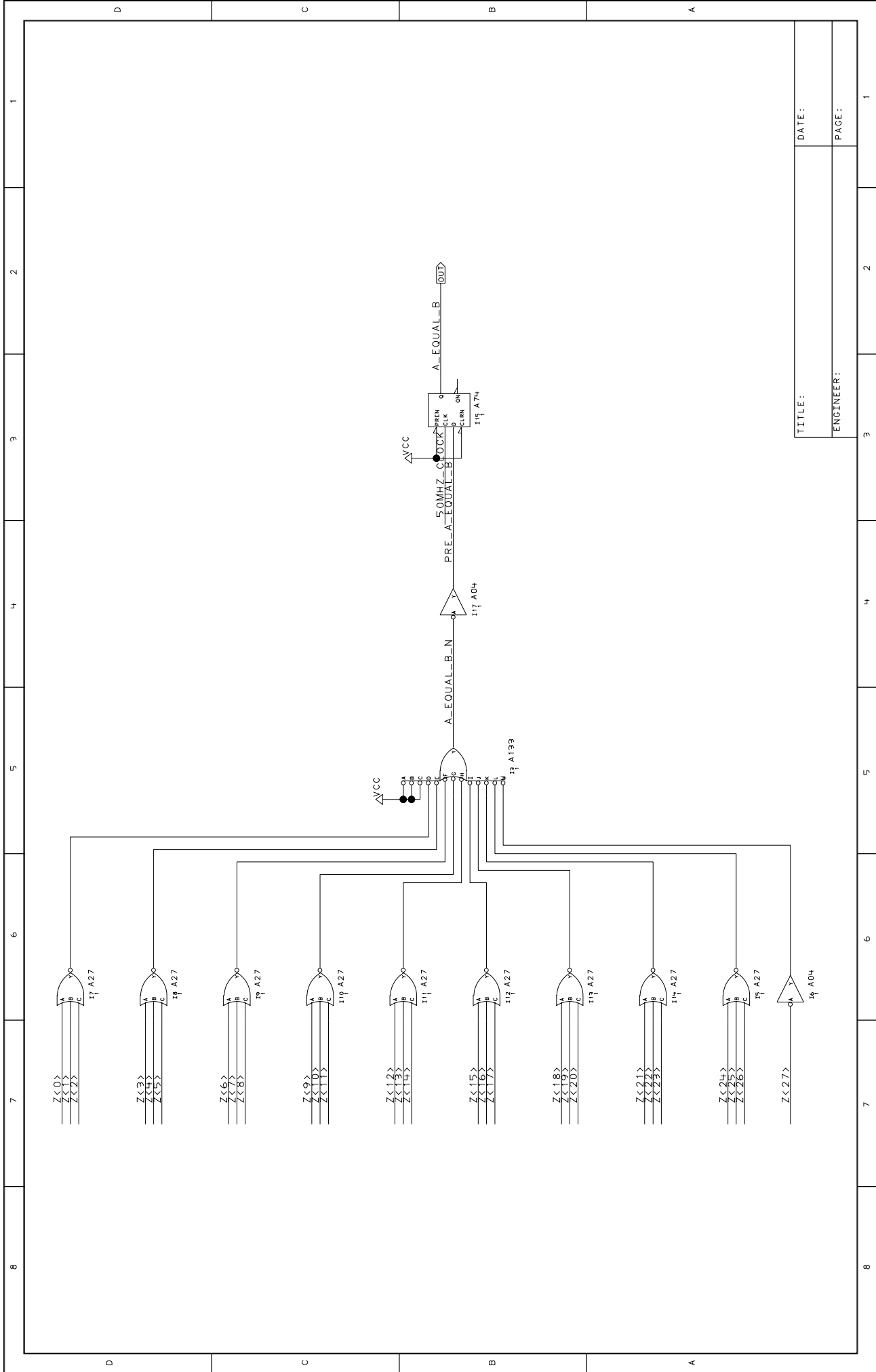
DATE: Fri Sep 25 14:19:13 2009
 DRAWING: LUNAR_TIMER.SCH.1.1
 ENGINEER: TIM VAN WECHEL
 PAGE: 1 OF 2



TITLE: LUNAR_TIMER
 DRAWING: LUNAR_TIMER.SCH.1.1.2
 DATE: Thu Sep 24 13:32:47 2009
 ENGINEER: TIM VAN WECHEL
 PAGE: 2 OF 2



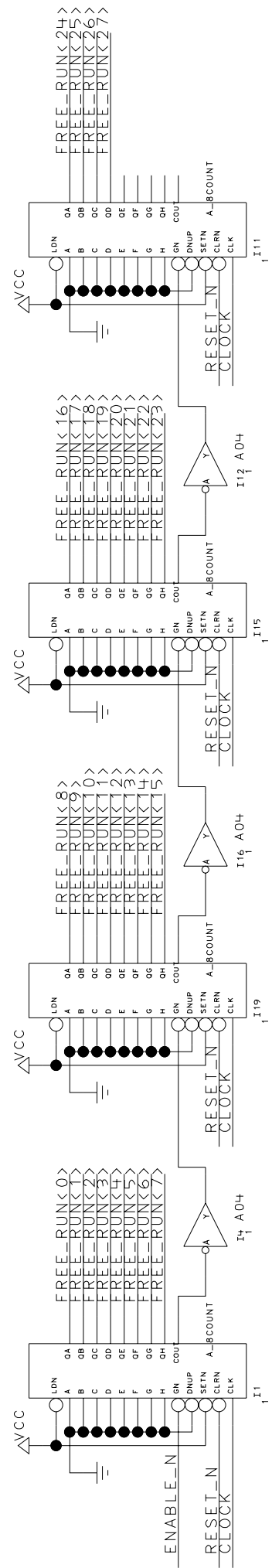
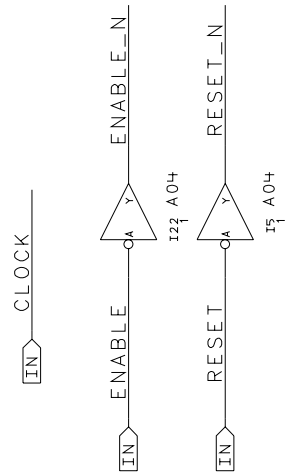
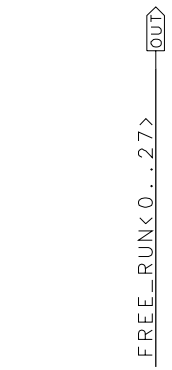
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 DATE: Thu Sep 24 13:32:38 2009
 ENGINEER:

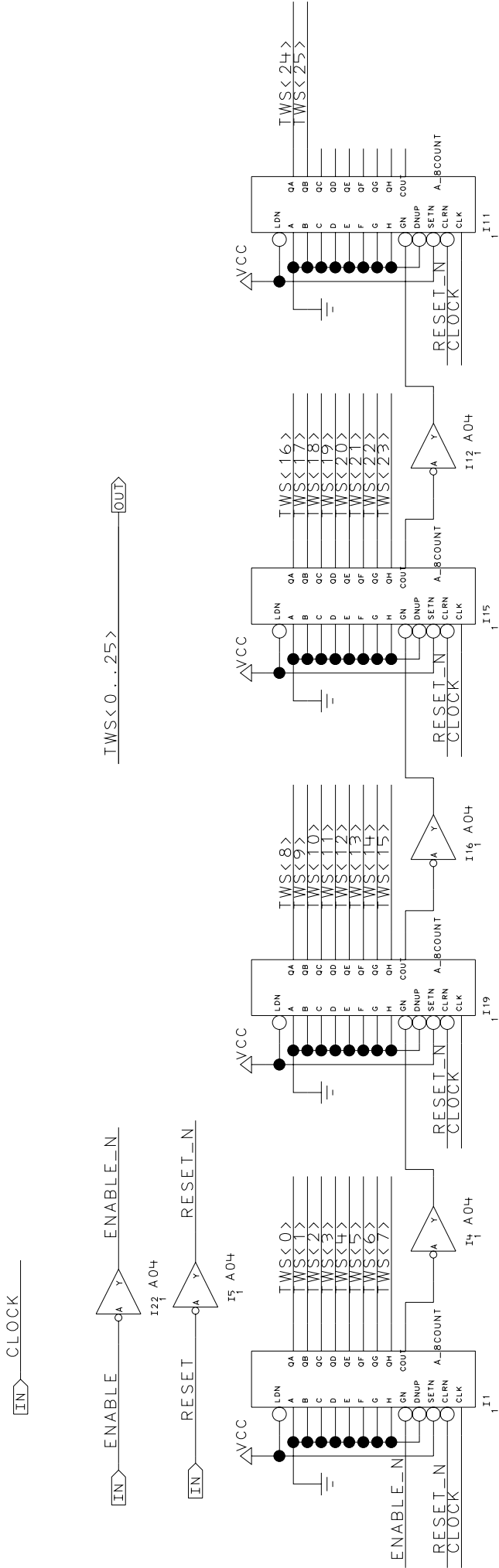


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ENGINEER:	PAGE:

DRAWING:
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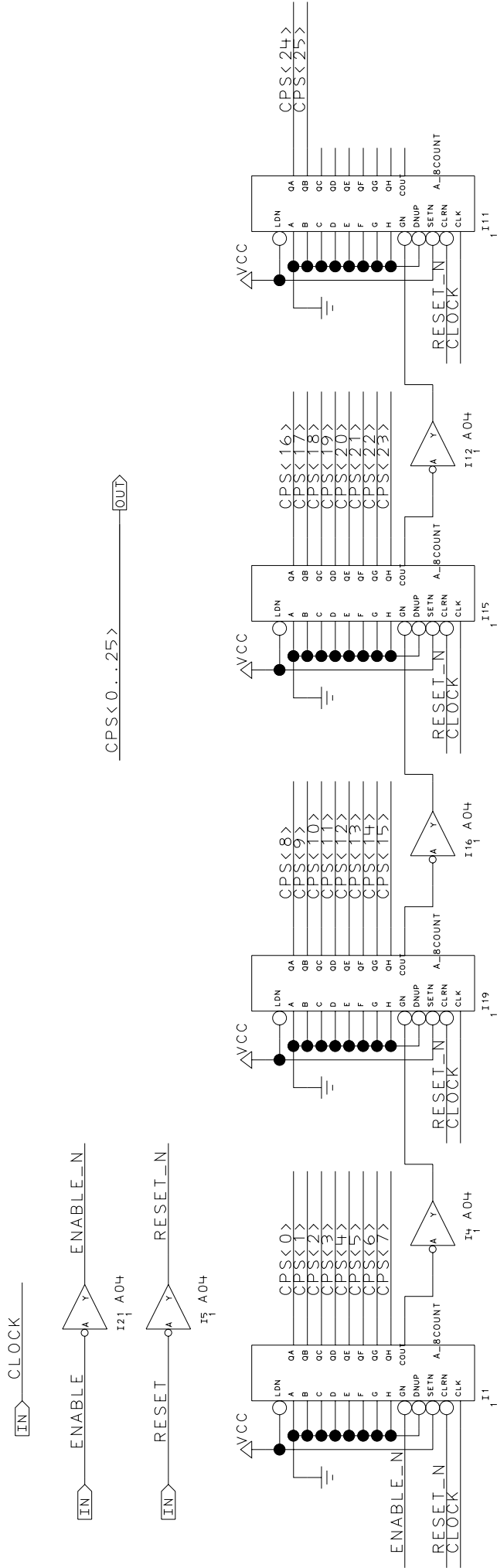
Thu Sep 24 13:32:40 2009





DRAWING:
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NO ABBREV

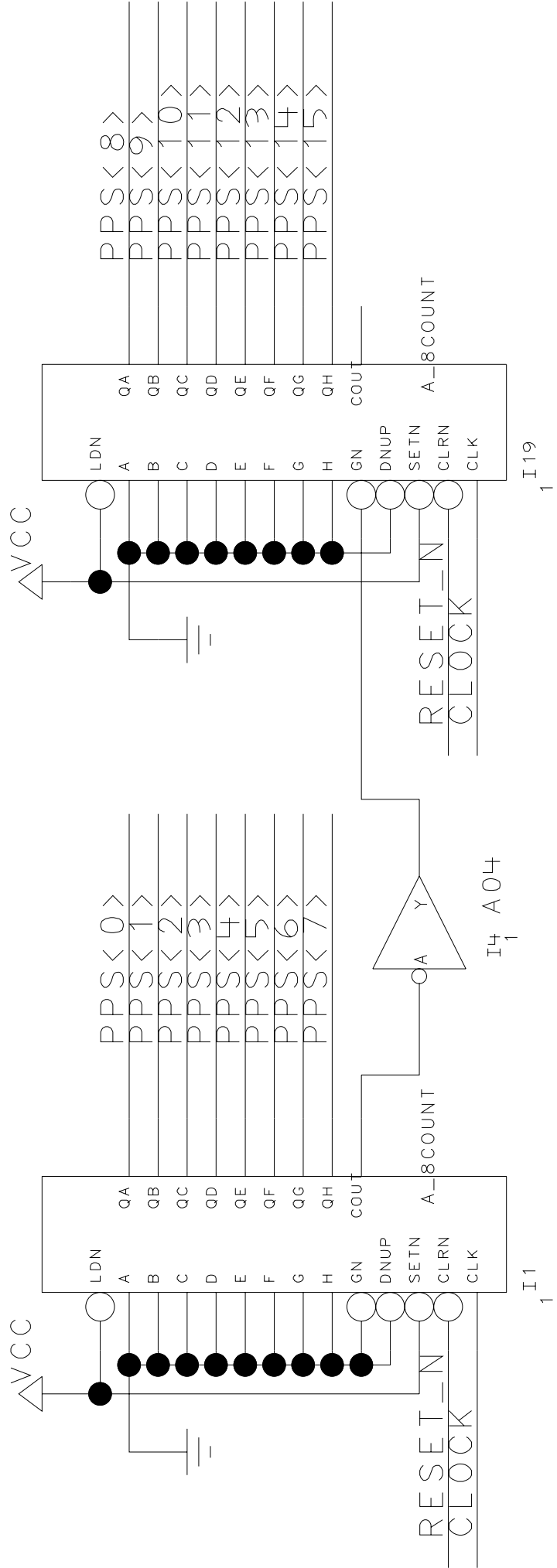
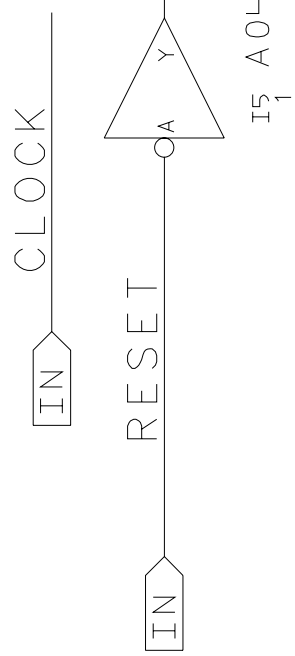
Thu Sep 24 13:32:44 2009



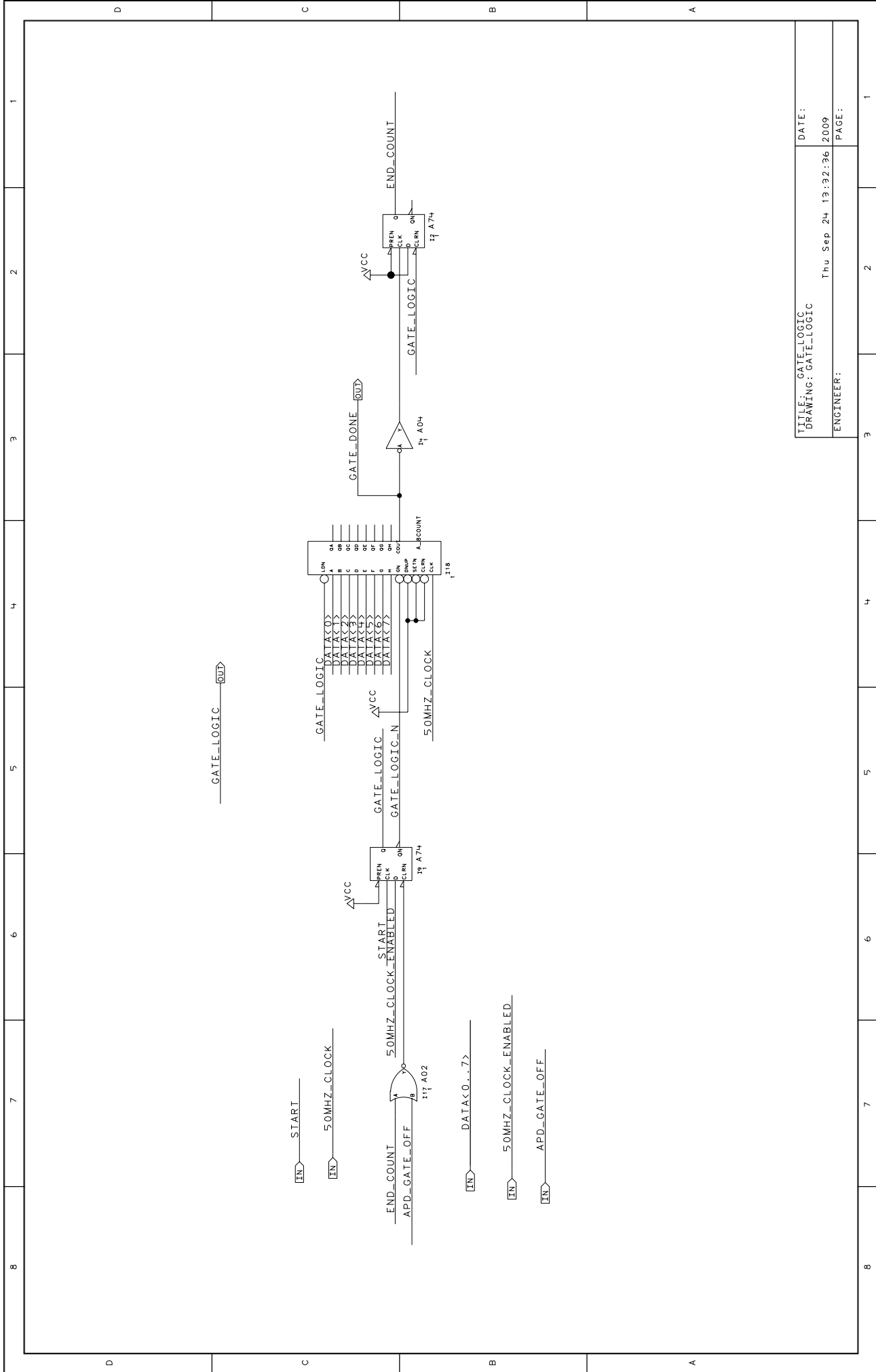
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Thu Sep 24 13:32:45 2009

PPS<0..15> OUT

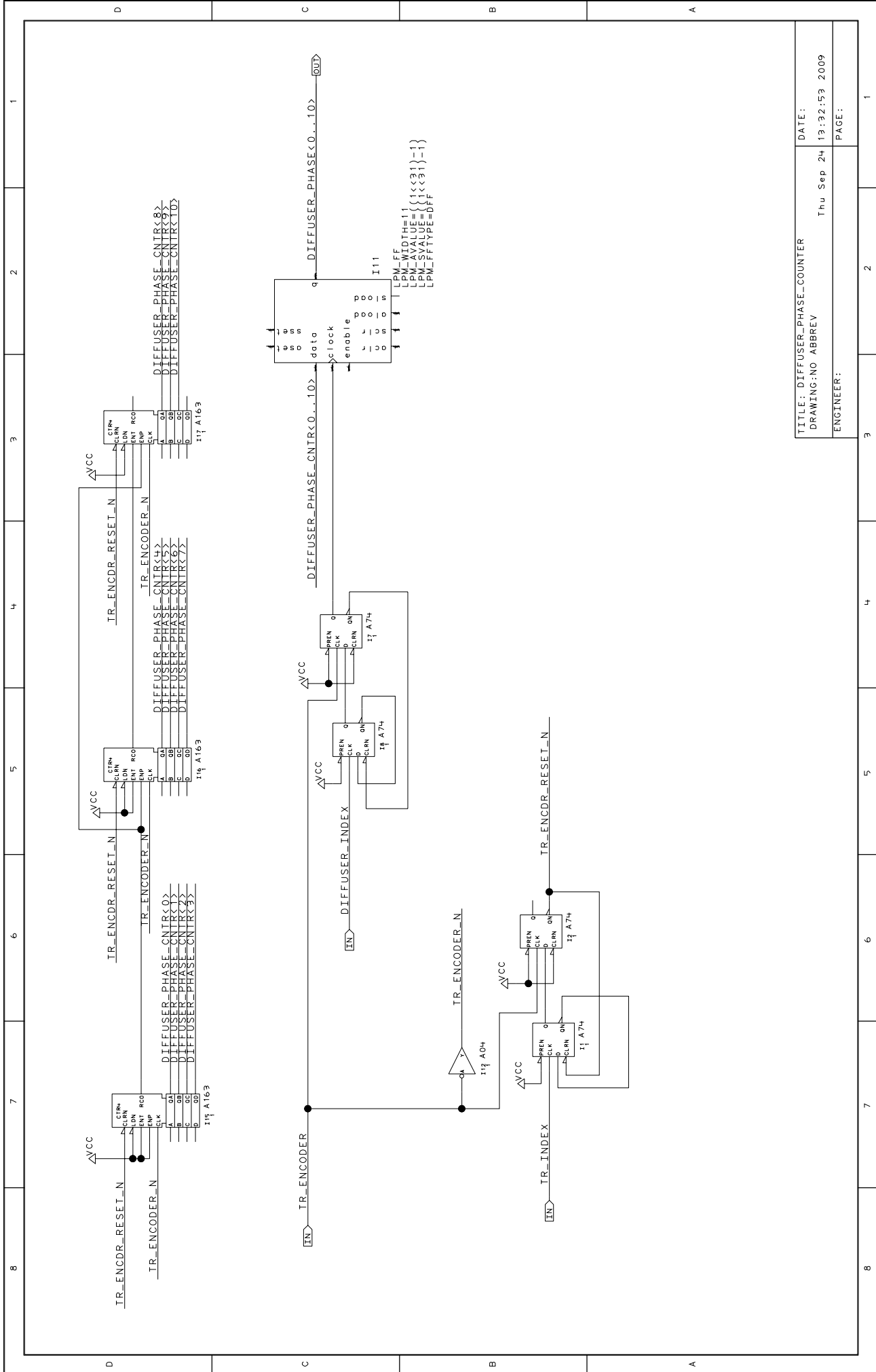


DRAWING :
PPS_COUNTER
NO ABBREV



TITLE: GATE_LOGIC
DRAWING: GATE_LOGIC
ENGINEER:
DATE: Thu Sep 24 13:32:36 2009
PAGE:

8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1



TITLE: DIFFUSER_PHASE_COUNTER		DATE:
DRAWING: NO ABBREV		Thu Sep 24 13:32:53 2009
ENGINEER:		PAGE:

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TR_ENCODER_RESET_N
TR_ENCODER_N
DIFFUSER_PHASE_CNTR<0>
DIFFUSER_PHASE_CNTR<1>
DIFFUSER_PHASE_CNTR<2>
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I1 A163

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I1 A163

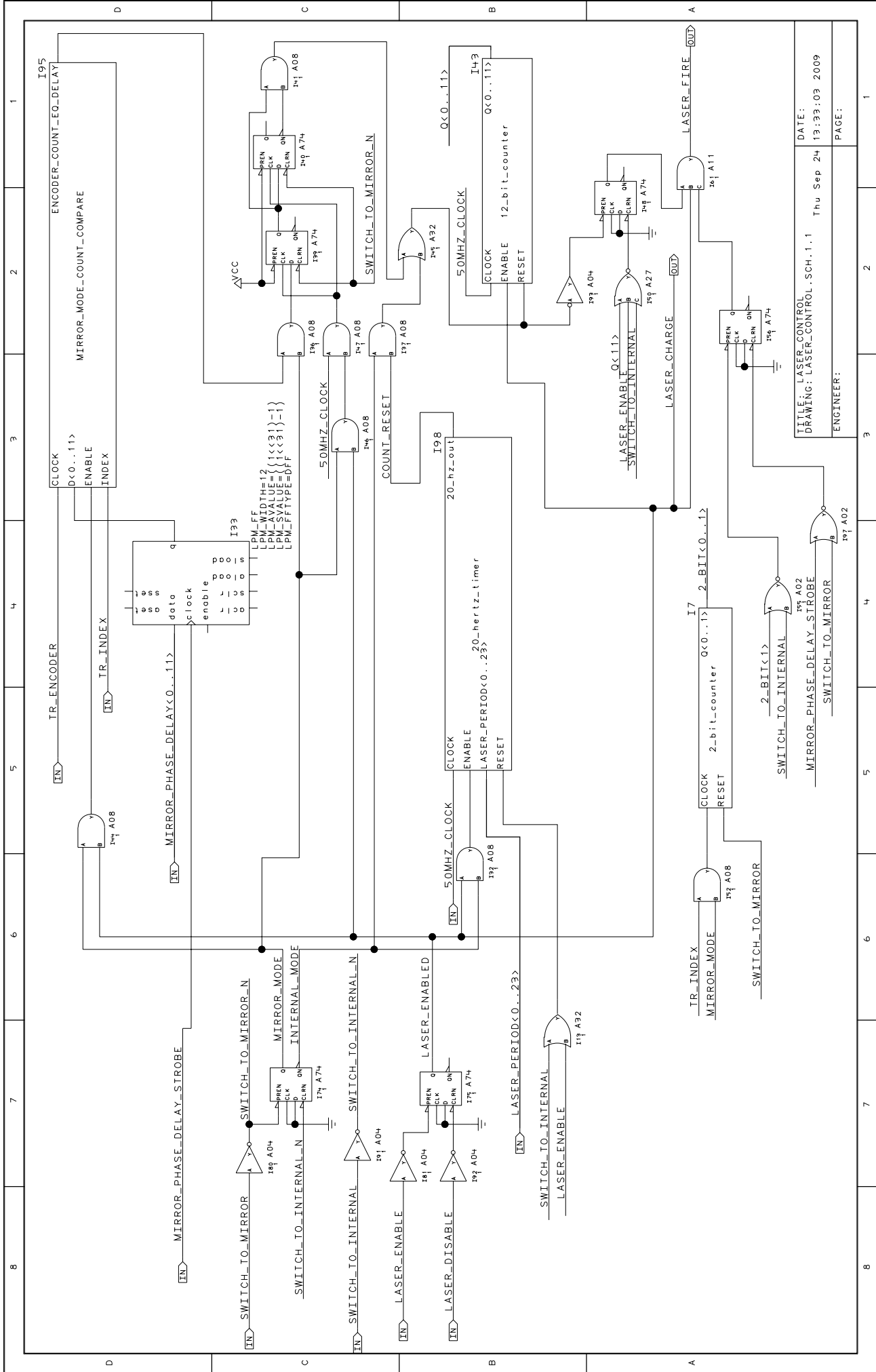
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I1 A163

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clock
enable
I11
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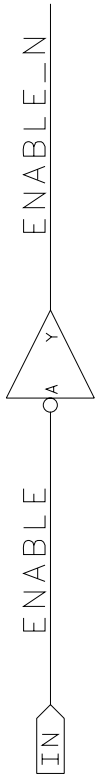
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I1 A74

IR_ENCODER_N
I1 A04
I1 A74

IR_ENCODER_RESET_N
I1 A74

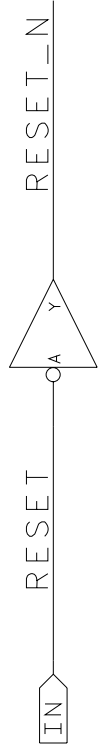
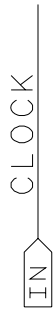


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DATE: Thu Sep 24 13:33:03 2009
ENGINEER:

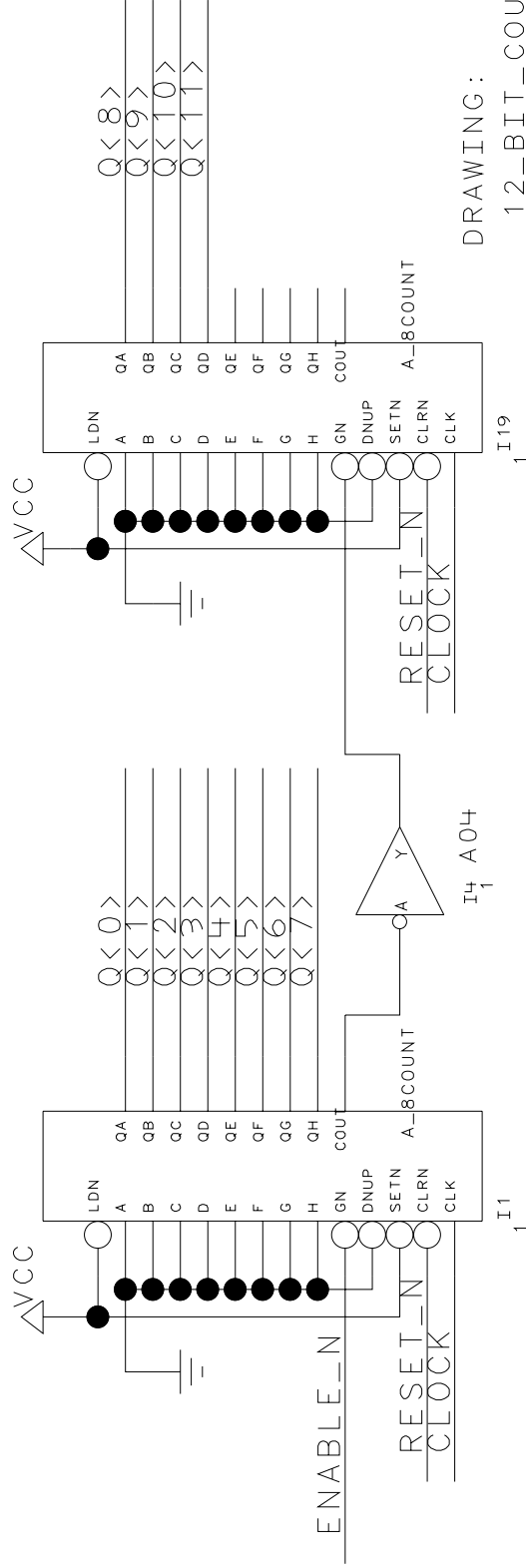


Q < 0 . . 1 1 > OUT

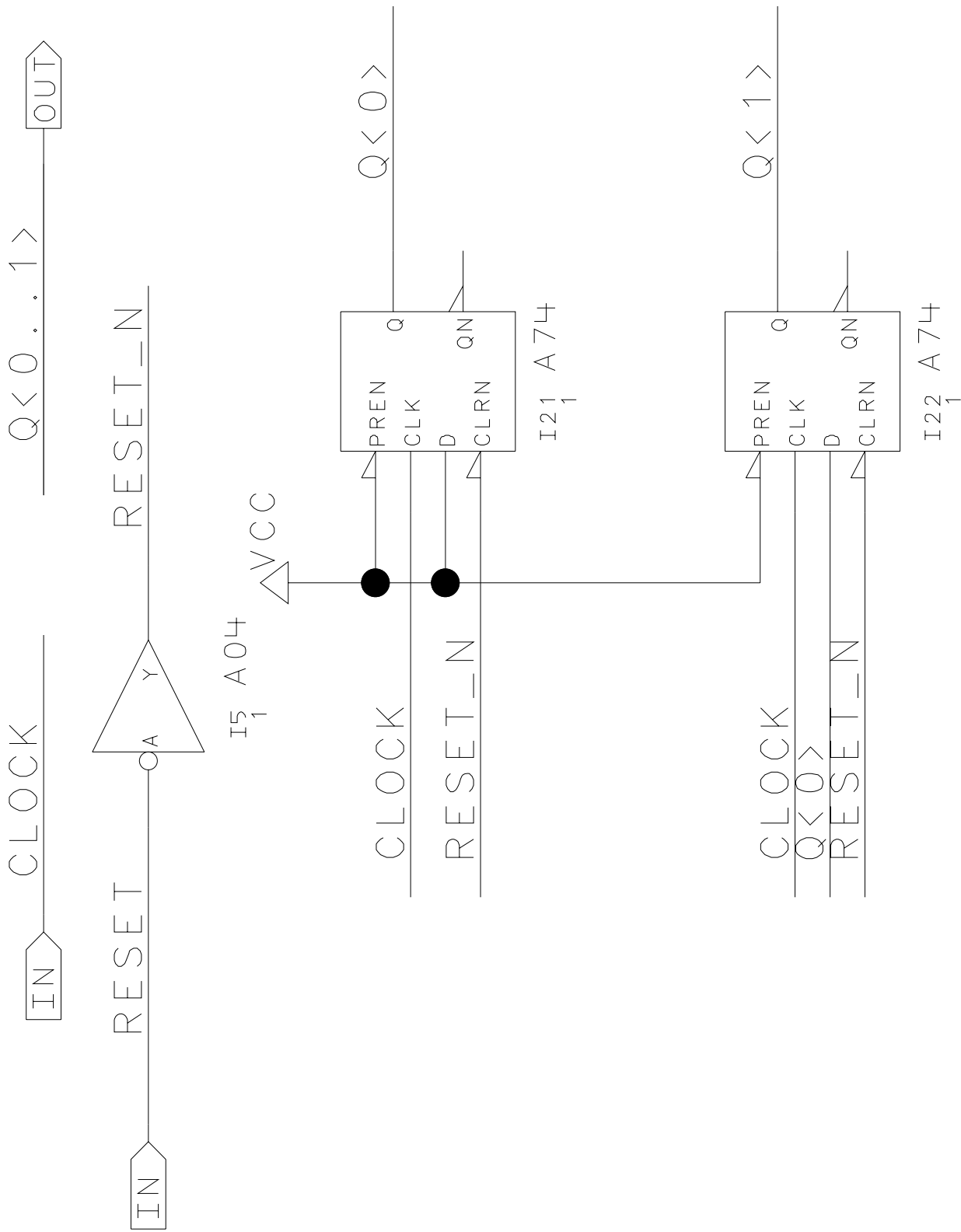
I21 A04



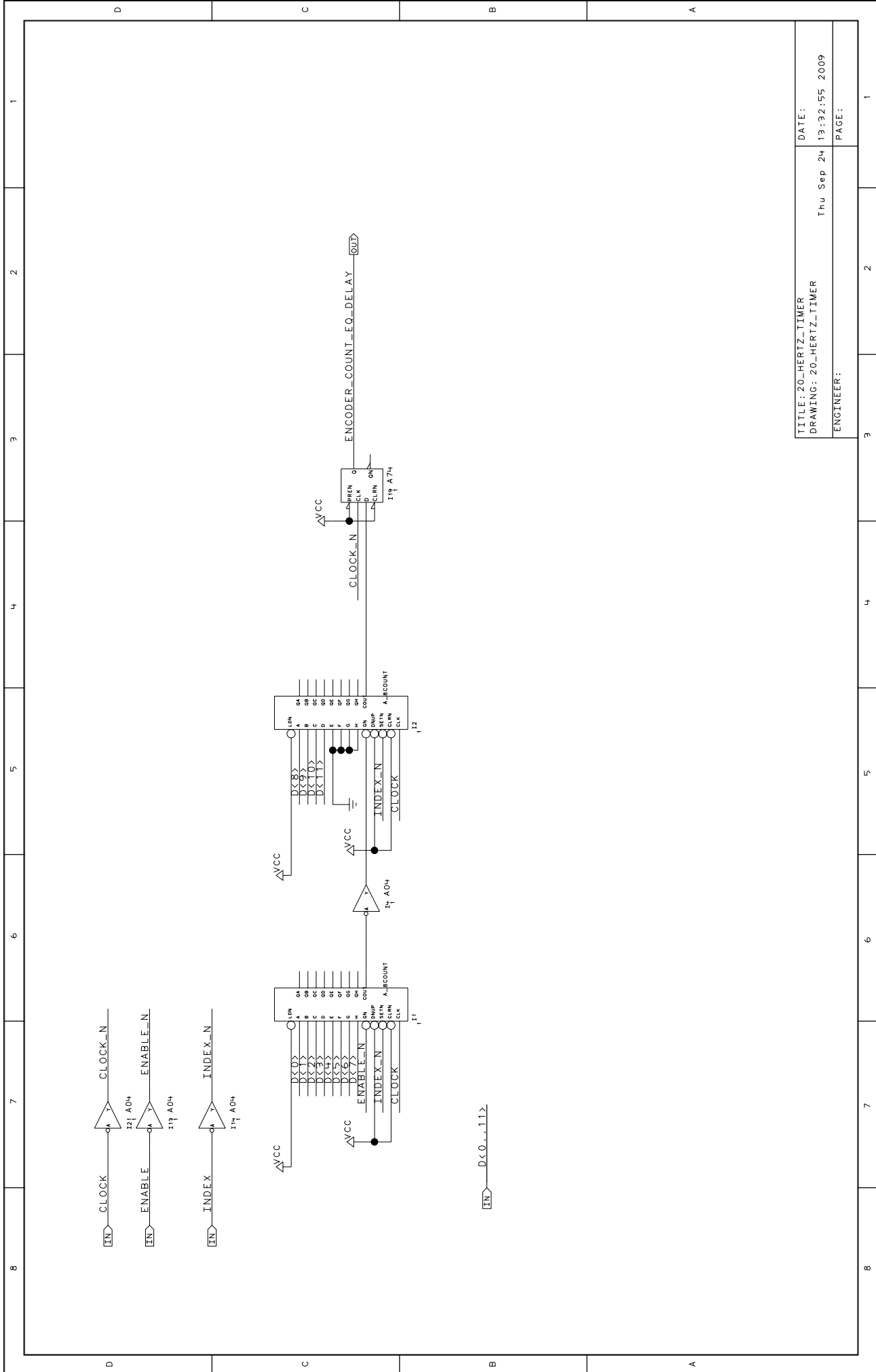
I5 A04



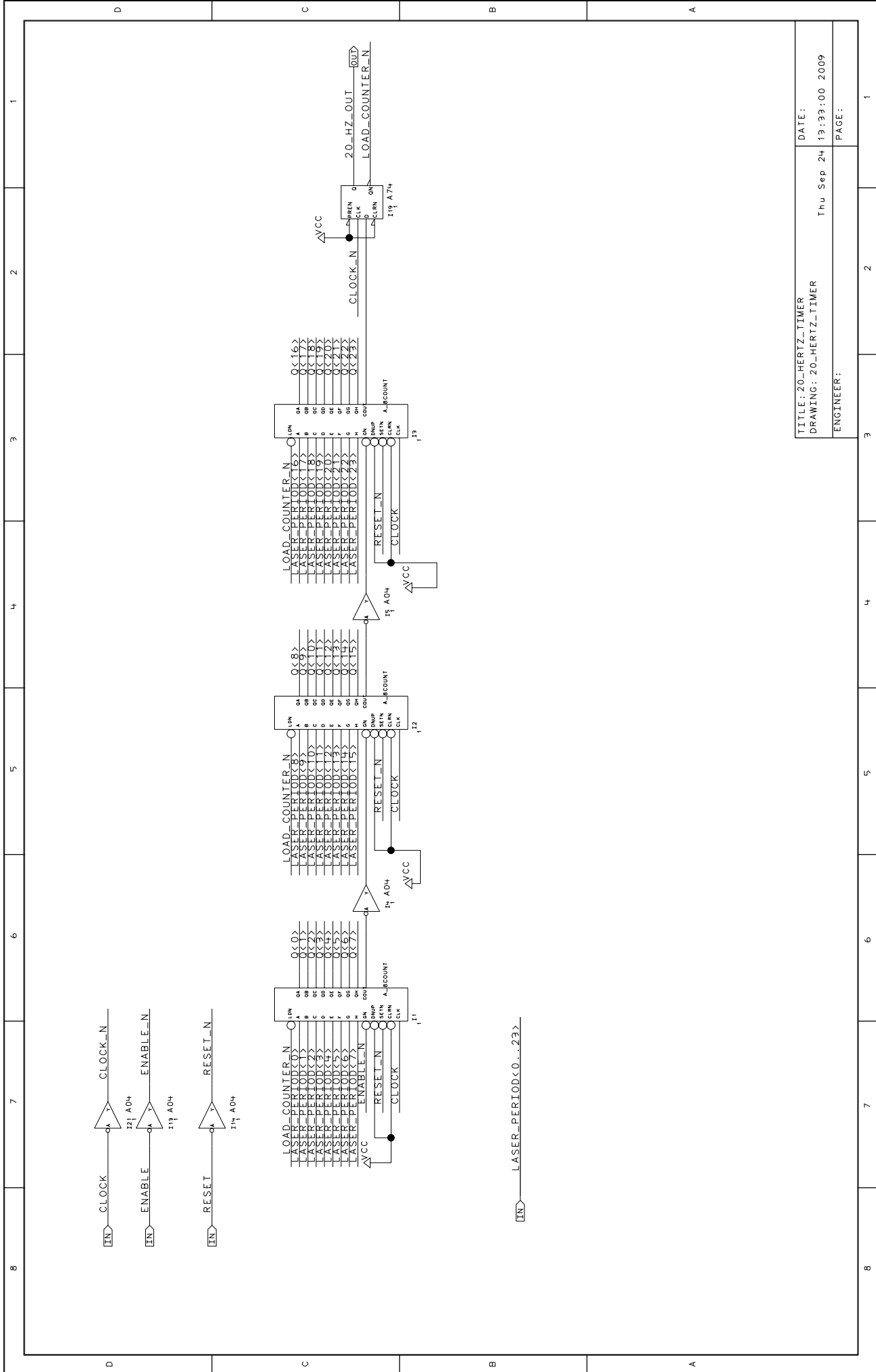
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12-BIT_COUNTER
NO ABBREV



DRAWING:
 2-BIT_COUNTER
 NO ABBREV

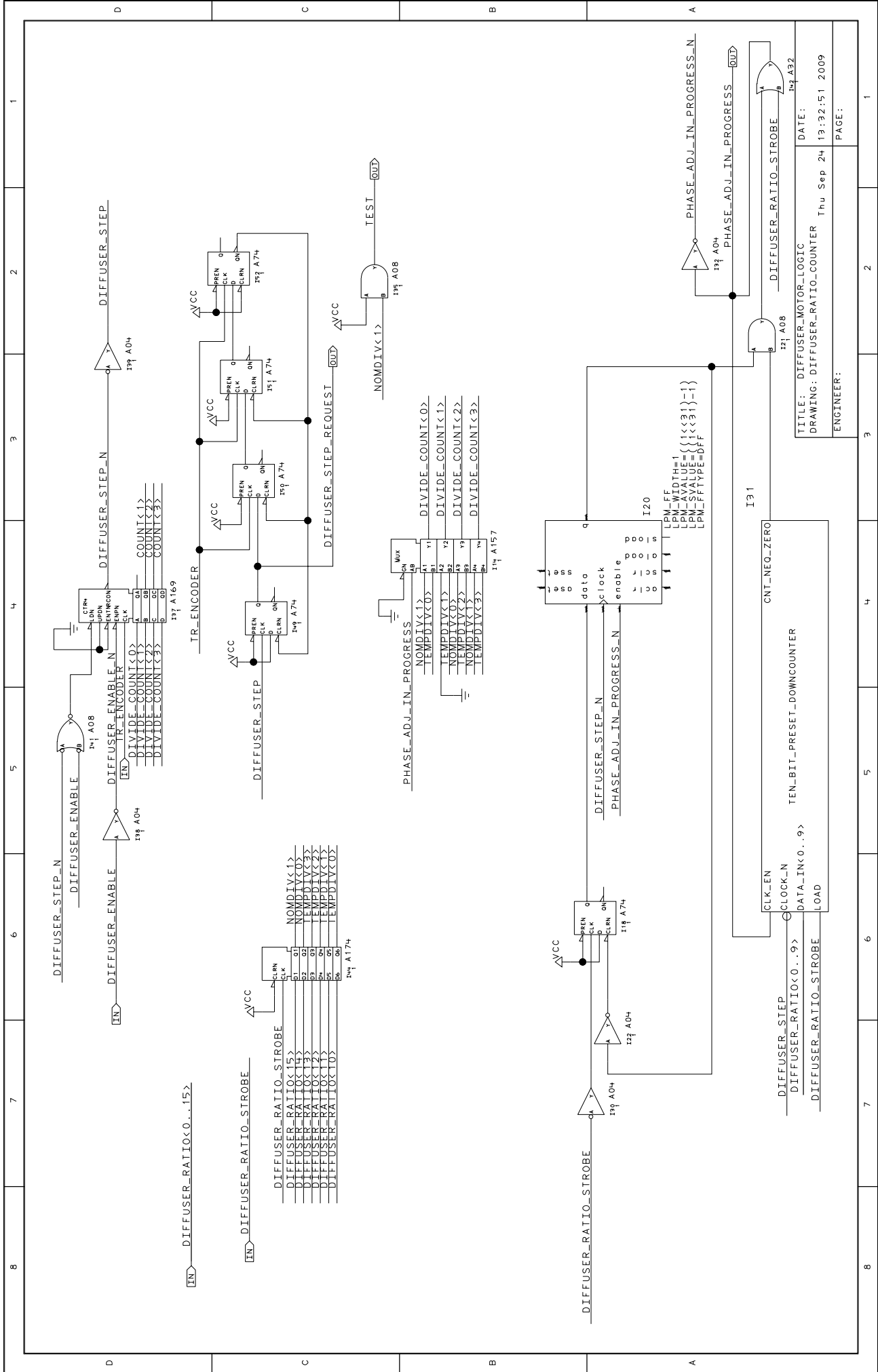


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DRAWING: 20-HERTZ-TIMER	Thu Sep 24 13:32:55 2009
ENGINEER:	PAGE:

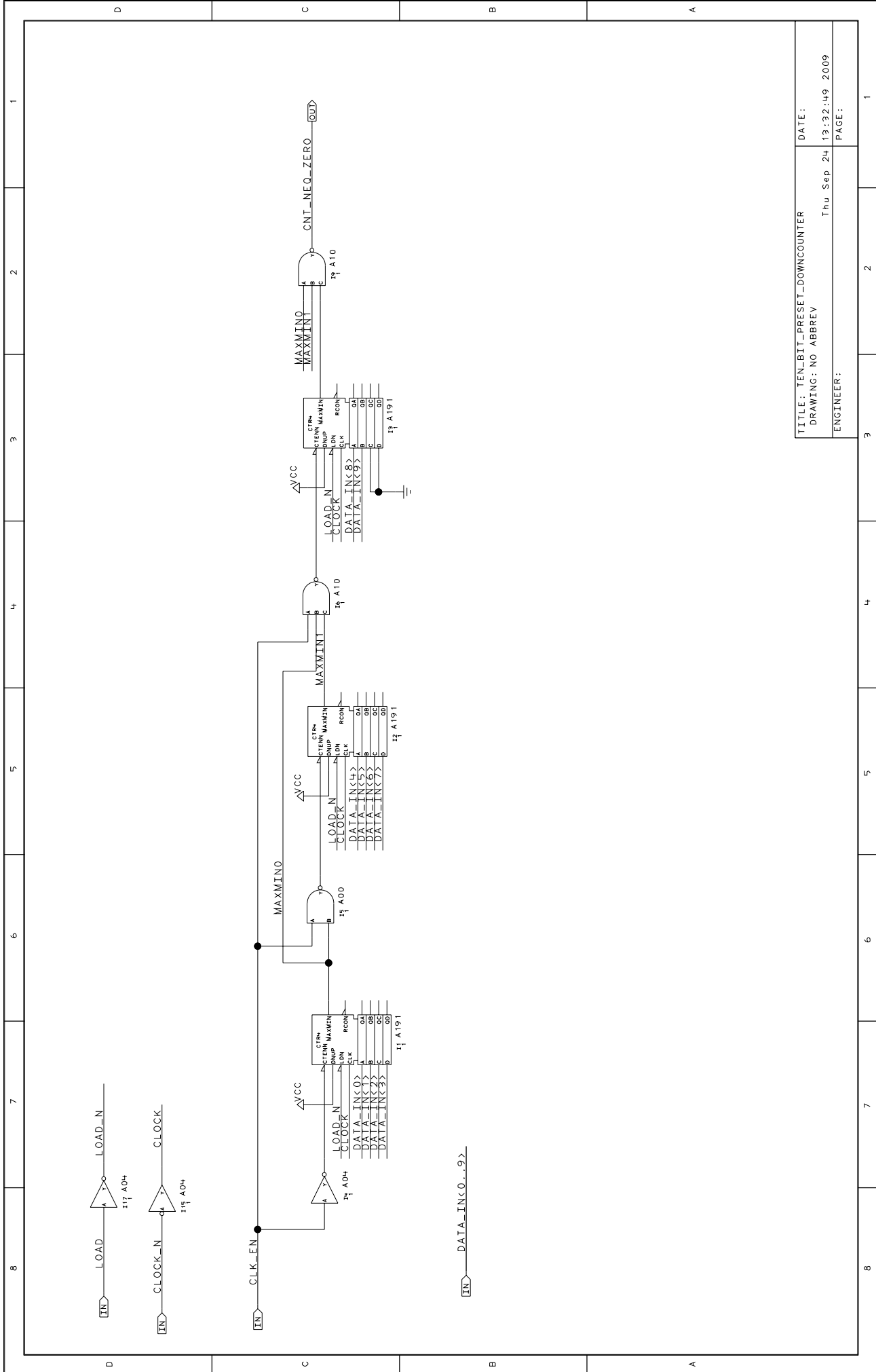


TITLE: 20-HERTZ-TIMER
 DRAWING: 20-HERTZ-TIMER
 ENGINEER:

DATE:
 Thu Sep 24 13:39:00 2009
 PAGE:



TITLE: DIFFUSER_MOTOR-LOGIC
 DRAWING: DIFFUSER_RATIO_COUNTER Thu Sep 24 13:32:51 2009
 ENGINEER:



TITLE: TEN_BIT_PRESET_DOWNCOUNTER	DATE:
DRAWING: NO ABBREV	Thu, Sep 24 13:32:49 2009
ENGINEER:	PAGE: