APOLLO Command Module

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1 The APOLLO Command Module (ACM)

The aptly named APOLLO Command Module (ACM) is a custom single-wide CAMAC module based on Altera programmable logic devices (PLDs). The ACM is responsible for timing, coordination, and various device controls. The ACM is based on two Altera chips, one of which interfaces to the CAMAC dataway and interprets NAF CAMAC commands and generates Look-At-Me (LAM) requests. The other Altera chip contains the timer, APD control, and laser fire control.

By implementing the ACM as a CAMAC module, we gain full computer control of ACM activities, and place this timing device right next-door to the critical TDC. The ACM also acts as the primary hardware interface to most of the rest of the system, so that it controls laser fire requests, laser safety, APD array protection, rotating optic phase, and diffuser/attenuator phase.

The ACM also provides a calibration service, so that the TDC may be checked with START/STOP pulses arriving precise multiples of 20 ns apart. The generation of START and STOP pulses is carried out by the Clock Slicer (formerly "Booster" board).

2 ACM Description

The APOLLO Command Module (ACM) is a highly versatile customized piece of equipment providing much of the smarts in the apparatus. The ACM is a single-slot CAMAC module based on a pair of Altera 7000AE series programmable logic devices (PLDs). These chips are separated into two functions. One handles the CAMAC dataway, interpreting addresses, function calls, read and write data, and sends LAM ("Look At Me") notices to the CAMAC controller. This chip can afford to be relatively slow, and has pretty simple innards, demanding only about 35% of the smaller 7256 chip (though larger physically, with 208 pins). The timing functions are contained on the "TIMER" PLD, clocked by the 50 MHz TTL from the Booster. The TIMER chip is full of many-bit counters, and as such demands the larger 7512 chip, though fewer I/O pins are needed. The TIMER PLD is capable of being clocked at speeds of < 116 MHz, and has an end-to-end propagation delay of ~ 7 ns. The slightly slower CAMAC chip is still high speed, with clocking up to 95 MHz and 10 ns propagation delay.

The Altera 7000 PLDs are re-programmable on the circuit board, so that we can in principle actually change the internal logic and functionality with the board in place in the CAMAC crate! To the extent that the hardware pinout and external connectivity is not changed, this allows versatility in the interface and internal logic scheme.

3 ACM Central Concept

The ACM employs a counter/register/comparator scheme to schedule gate events. In other words, the value of a counter, clocked at 50 MHz, is compared against a pre-loaded register containing some data value.

When these match, an action is taken. For example, in scheduling the lunar gate, the free-running counter (FRC) is compared against a value—set on each shot by software—that we know the FRC will reach when the lunar photons are about to return. This value has been loaded into the ACM, having been derived from a polynomial prediction using the time of laser fire as the time input to the polynomial. When the FRC reaches the prescribed value, the APD gate is turned on. The mechanism for setting the width of the APD gate works in a similar way. When the gate is turned on, a counter is reset. When this counter reaches a count that equals a preset and pre-loaded data value (the width parameter), the gate is commanded to turn off. At each gate closing, the FRC value is latched so that it may be read out (though the FRC counter keeps counting uninterrupted). Likewise, the time-within-second counter—which is reset once per second—is latched so that the time of the gate may be known to 20 ns precision.

Stare mode refers to a mode wherein the FRC is reset after it reaches the FRC delay set (thus opening a LUN-type gate). Because it is reset, it will reach the delay count again in the same amount of time, repeating the cycle. So this becomes a way to run a series of gates at a selectable period, making this a convenient way to "stare" at the sky, a star, etc. No FID-type gates are generated, only LUNs.

4 ACM Front Panel

The ACM front panel takes a number of inputs and provides a number of outputs, described here. The single-width panel accommodates 22 LEMO connectors at a 0.30-inch spacing. LEDs to the sides of the connectors indicate functionality.

The bottom five connectors on the ACM are labeled as input/output lines. These are jumper-configurable to act either as outputs or inputs to the Altera TIMER chip. At present (Nov. 2010), the Altera chip is programmed to have 1, 2, 3, and 5 act as outputs, while 4 is an input. The outputs work so that CAMAC commands can set them to a TTL high state or low state (default). The input can read logic high or logic low. The tables below indicate ipermanent and temporary input/output assignments.

4.1 Inputs

Logic Name	Front Panel	Signal Type	Connects To:	Action
CLOCK	CLK	50 MHz square	Booster Clock	ACM time ref.
PPS	1 PPS	20 μs TTL	XL-DC 1 PPS	alerts new second
PHOTODIODE	PIN	100 ns TTL	9327 TTL out	alerts laser fire
DIFF_INDEX	CAL	~ 4 kHz TTL	diffuser opto-isolator	1 per revolution
TR_INDEX	IDX	$\sim 50\,\mu$s TTL	T/R opto-iso index	1 per revolution
TR_ENCODER	ENC	~ 40 kHz TTL	T/R opto-iso encoder	TR_ENCODER
STATUS<0>	I/O 4	TTL	interlock (TBD)	interlock state

The first three inputs are terminated in 50 Ω, while the last four are terminated in 4 kΩ.

4.2 Outputs

Logic Name	Front Panel	Signal Type	Connects To:	Action
LUN_START	LUN ST	20 ns TTL	Booster START	slices START pulse
CAL_START	CAL ST	20 ns TTL	—	on FID gate open
GATE_START	OPN	20 ns TTL	—	on any gate open
GATE_DONE	CLS	20 ns TTL	—	on gate close
STOP	STOP	20 ns TTL	Booster STOP	slices STOP pulse
GET_TIME	TME	160 ns TTL	XL-DC trig in	latch GPS time
APD_GATE_LOGIC	GTE	$N \times 20$ ns TTL	—	mimics gate
EN_APD_GATE	APD	$N \times 20$ ns TTL	APD gate input	turns on APD
LASER_CHARGE	LSR	DC TTL	laser "externals"	tells caps to charge
LASER_FIRE	ZAP	40 μs TTL	laser "externals"	tells laser to fire
LASER_BLOCK	BLK	DC TTL	interlock	shutters laser output
DIFFUSER_STEP	I/O 1	~ 4 kHz TTL	diffuser opto-iso	drives diffuser motor
I/O 2	I/O 2	DC TTL	FPD Faker Box	switch Ortec input
I/O 3	I/O 3	DC TTL	TDC window jmpr	Change TDC gate width
POWER_METER	I/O 5	DC TTL	flip dichroic	illuminates pwr meter

All outputs are capable of driving 50 Ω termination. The LUN_START occurs only at the beginning of a lunar gate, and it is this that requests a START clock pulse from the Booster when the calibration mode is enabled. The STOP signal and GATE_DONE signal are identical: both occur at the end of a gate. The APD_GATE_LOGIC and EN_APD_GATE are effectively identical, though the former activates for every gate event, while the latter is onnly activated if the APD drive is enabled.

In addition to these outputs, various LEDs indicate the status:

- An orange "N" light blinks when the module is being addressed via CAMAC commands.
- A green LED blinks at one pulse per second to indicate clock heartbeat.
- A blue-white LED blinks with the APD gate logic to indicate gate action.
- A yellow LED indicates the APD drive is enabled, and thus follows the gate logic.
- A green LED indicates that the laser is enabled.
- A blue-white LED flashes when a laser fire request is issued.
- A red LED indicates that the laser is unblocked and able to fire at the sky.

5 ACM Commands

The ACM commands take the form of CAMAC NAF commands (N = slot number; A = address, F = function), and follows standard CAMAC numbering conventions. A complete list of the commands is included below. Here, we summarize the commands in an abbreviated form, the intention being to flesh out the functionality of the ACM. In the following, FRC means free-running counter, TWS means the time within second counter, CPS is the counts-per-second counter, and a LAM is a look-at-me interrupt request.

5.1 Reading Data

Upon the GATE_DONE signal, the FRC and TWS counters are latched, and each of these can be read out. Upon the 1 PPS signal, the CPS and accumulated second counters are latched, and these can be read out. The T/R encoder counts between the T/R index and diffuser index indicates the diffuser motor phase, and can be read out. The value set fo the gate width and the value stored as the FRC delay can be read.

5.2 Writing Data

The following data can be written to the ACM: delay setting (comparison trigger value) for the FRC; gate width parameter; T/R mirror phase delay (at what phase mirror fires); laser fire period for internally generated firing; phase adjustment parameters for modifying the diffuser phase.

5.3 Setting States

Various commands exist for clearing registers and LAMs. The 50 MHz counters can all be reset. The accumulated seconds counter can be reset. The APD gate can be commanded to the off position. In addition, the following state changes can be made. In what follows, the default state (happens on CAMAC initialization command) is the first listed, the alternate state indicated after the slash.

Stare mode can be disabled/enabled. The APD drive can be disabled/enabled. All 50 MHz counters can be disabled/enabled. The laser drive can be disabled/endabled. The laser shutter can be blocked/unblocked. The LUN_START output can be disabled/enabled—when enabled, the Booster processes START pulses that are used in TDC calibration. The laser fire mode can be switched to internal pulse-train generation or T/R encoder drive. Each of the I/O outputs (2, 3, 5) can be set to low/high states.

LAMs can be configured to fire on lunar gates, fiducial gates, GATE_DONE (all gates) via a LAM mask. The LAM status can be read, as well as LAM request (those LAMs enabled by the mask). LAMs can be software-generated, which can be useful in verifying LAM operation and response.

5.4 Command Set

Following is a list of the CAMAC-actuated ACM commands in A(x)F(x) form, with brief descriptions.

A	F	Function Description
0	0	Read lower 16 bits of free-running counter (FRC)
1	0	Read upper 12 bits of free-running counter (FRC)
2	0	Read lower 16 bits of time-within-second counter (TWS)
3	0	Read upper 10 bits of time-within-second counter (TWS)
4	0	Read lower 16 bits of counts per second (CPS)
5	0	Read upper 10 bits of counts per second (CPS)
6	0	Read accumulated seconds counter
7	0	Read diffuser motor phase
0	1	Read lower 16 bits of FRC delay set
1	1	Read upper 12 bits of FRC delay set

2	1	Read gate width set value: return is 256*FID_WIDTH + LUN_WIDTH
3	1	Read STATUS bit (I/O 4 input; ultimately reflecting interlock)
4	1	Read hardware (2 bits)/firmware (6 bits) version, arranged: hhffffff
12	1	Read LAM status (1=FID, 2=GATE_DONE, 4=LUN), enabled or not
13	1	Read LAM mask (1=FID, 2=GATE_DONE, 4=LUN)
14	1	Read LAM request (1=FID, 2=GATE_DONE, 4=LUN), live LAM
15	1	Read Gate type: 0=FID, 1=LUN
15	8	Test LAM (returns status on Q: Q=0 if no LAM, Q=1 if LAM set)
0	9*	Clear group 1 registers (data values: FRC, TWS, CPS, PIN)
0	10	Clear LAM status register
0	11*	Clear group 2 registers (set values: FRC delay, gate width)
1	11*	Clear groups 1 & 2 registers
2	11	Clear LAM status register; Clear group 1 registers
3	11	Clear LAM status register; Clear groups 1 & 2 registers
0	12	Reset accumulated seconds counter
1	12	Reset all 50 MHz counters
2	12	Reset accumulated seconds and 50 MHz counters
3	12*	Disable Stare mode (enable normal ranging mode)
4	12	Enable Stare mode (for looking at stars, background)
0	13	Request APD gate OFF
1	13*	Disable APD drive (logic still goes, but APD drive disabled)
2	13	Enable APD drive
3	13*	Disable 50 MHz clock
4	13	Enable 50_MHz clock
5	13*	Disable Laser drive (ACM can’t fire laser)
6	13	Enable Laser drive (ACM allowed to fire laser)
7	13*	Block laser beam
8	13	Unblock laser beam
9	13*	Disable START pulse request via LUN_START output

10	13		Enable START pulse request via LUN_START output
11	13*		Switch laser fire mode to internal 20 Hz generator
12	13		Switch laser fire mode to T/R switch (external) drive
13	13*		Disable diffuser step counter
14	13		Enable diffuser step counter
2	14*		Set I/O 2 output low; FPD input to Ortec 9327
3	14		Set I/O 2 output high; fake signal input to Ortec 9327 (fakerun)
4	14*		Set I/O 3 output low; set TDC for 100 ns gates
5	14		Set I/O 3 output high; set TDC for 800 ns gates
8	14*		Set I/O 5 output low; laser bolometer out
9	14		Set I/O 5 output high; laser bolometer in
0	17	*data*	Write lower 16 bits of delay data for FRC
1	17	*data*	Write upper 12 bits of delay data for FRC
2	17	*data*	Write gate width set data; applies to both LUN and FID gates
3	17	*data*	Write mirror phase delay
4	17	*data*	Write lower 16 bits of internal laser fire period
5	17	*data*	Write upper 10 bits of internal laser fire period
6	17	*data*	Write diffuser phase adjust command
7	17	*data*	Write gate width for FID gates
12	19	*mask*	Set LAM status (1=FID, 2=GATE_DONE, 4=LUN) simulate LAM
13	19	*mask*	Set LAM mask (1=FID, 2=GATE_DONE, 4=LUN)
0	20		Strobe FRC delay write (transfer all 28 bits to timer chip)
1	20		Strobe internal laser fire period
2	20		Reserved Strobe
3	20		Reserved Strobe
12	23	*mask*	Clear LAM status
13	23	*mask*	Clear LAM mask
*			Happens on Initialize (Z) command