APOLLO Timing Scheme

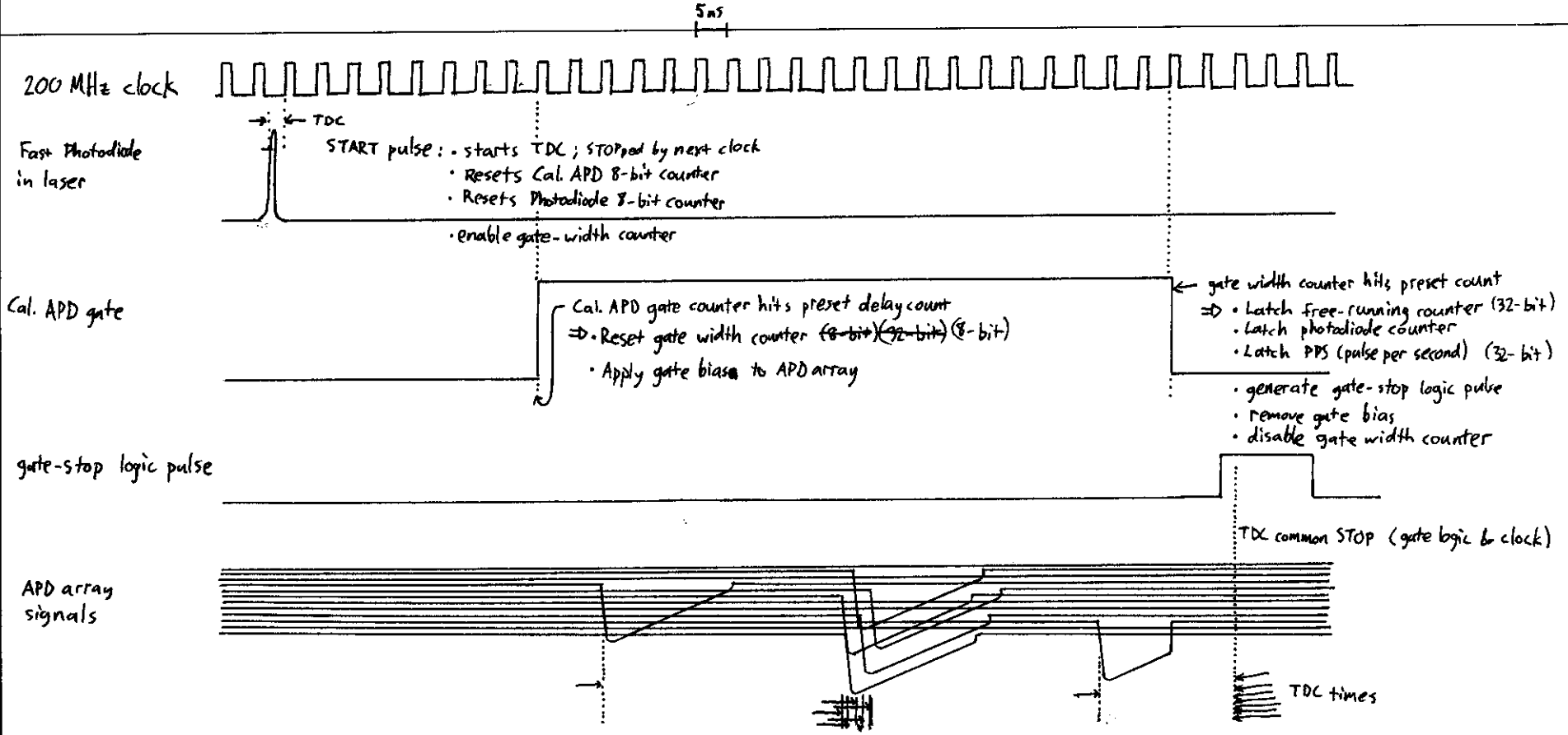
The proposed APOLLO timing scheme utilizes the following equipment

- Control computer that drives laser (via mirror), computes timing parameters, acquires data
- True-time GPS-slaved clock @ 50-200 MHz, few ps jitter, 40 ns accuracy
- Bank of TDC Units: Phillips Sci. 7186 has 16 channels, 20 ps RMS jitter, 25 ps resolution, 12-bit
- Gating / Timing circuit, largely counter based, PAL-friendly, flexible

The scheme goes something like this:

- The computer, knowing when laser last fired, computes (looks up) distance to moon at that time (plus one-way delay) – varies by $\leq 3\,\mu s$/sec – & computes mirror rate & delay
- The computer issues rate to mirror, loads delay into FIFO buffer
- Resolver on mirror motor tells laser to fire
- Fast Photodiode in or near laser senses fire; START to TDC; Resets photodiode counter and calibration gate counter. Next clock pulse STOPs TDC
- After ~50 ns delay, gate counter hits preset value; Resets gate width counter, applies bias gate to APD, enables gate-width comparator
  - Any detected photons START corresponding TDC channel
  - Gate-width counter reaches prescribed count, shuts off APD bias, generates gate-stop logic pulse, Latches free-running, PPS, and photodiode counters
  - Gate-stop logic AND clock provide common STOP to TDC
  - Gate-stop logic alerts computer to newly available data (TDC, latched counters)
- Computer loads register with time for next gate, in units of free-running counter.
- When free-runner reaches prescribed value, gate-width counter is reset, gate width comparator enabled, APD biased on. Double-bullet items followed from top-down
  - Back to beginning bullet

- 1 PPS output of True-time clock resets the PPS 32-bit counter and latches the CPS (counts per second) 32-bit counter. PPS enables determination of where within second events occur, and CPS serves to verify all clock pulses accounted



gate-stop logic pulse alerts computer to new data: Computer gets all TDC outputs; reads registers: photodiode, free-runner, PPS, CPS, delay knob

Computer loads register with time for next gate, accounting for delay knob value (allows manual slew in time)
When free-running counter reaches prescribed count, gate width counter is reset, APD gate bias applied, followed by identical pattern as above

Additionally, the 1PPS output of the clock latches the CPS (counts per second) ~~register~~ counter (32-bit), then resets the PPS & CPS counters
(or lets the CPS free-run)

Need for 200 MHz goes away with this scheme & Phillips Sci 7187 TDC

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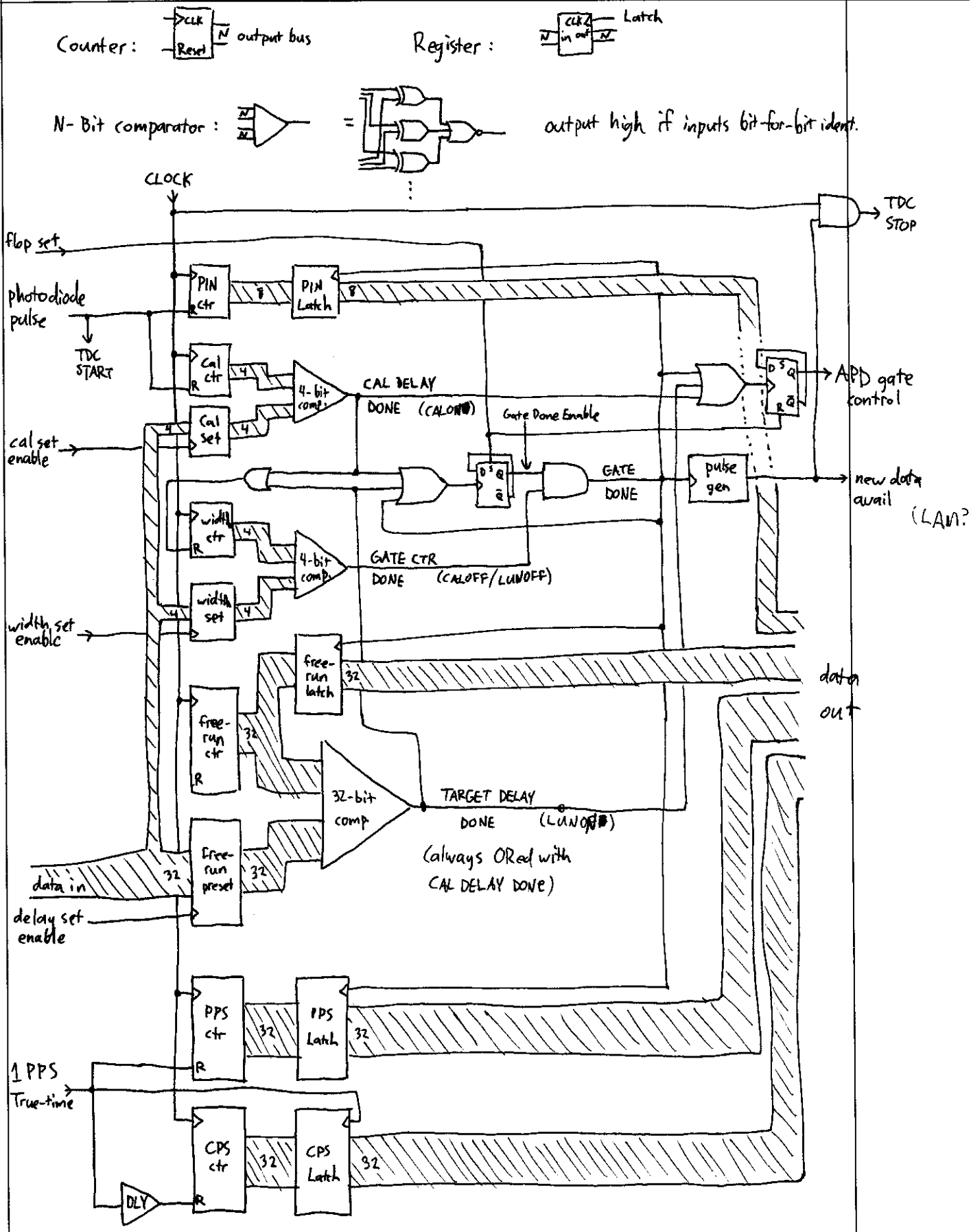
Counter :
CLK
Reset
N
output bus
Register :
clk
in
out
Latch
N- Bit comparator :
output high if inputs bit-for-bit ident.
CLOCK
TDC STOP
flop set
photodiode pulse
TDC START
PIN ctr
PIN Latch
Cal ctr
Cal set
4-bit comp
CAL DELAY DONE (CALON)
Gate Done Enable
APD gate control
cal set enable
GATE DONE
pulse gen
new data avail
(LAN?
width ctr
width set
GATE CTR DONE (CALOFF/LUNOFF)
width set enable
free-run latch
data out
free-run ctr
32-bit comp
TARGET DELAY DONE (LUNOFF)
Always ORed with CAL DELAY DONE)
data in
free-run preset
delay set enable
PPS ctr
PPS Latch
1 PPS True-time
CPS ctr
CPS Latch
DLY

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The proposed control/timing scheme allows the following CONTROL OPTIONS:

- We can rotate the mirror at a speed such that the lunar return always arrives at the same time relative to laser pulses — say 20 ms after each firing (themselves 50 ms apart).

  This is accomplished by dividing the round-trip time by 20 Hz, rounding to the nearest N.4 rotations ($N \sim 50$), re-computing the rate to feed to mirror.

  For satellites, $N=0$, so we'll have to take what we're given — 2+ ms for low-earth, 40+ ms for LAGEOS.

- We can have a "knob slew" option that adds a manually variable delay to the return gate for rapid interactive searching (essential option)

- The computer can perform an automated temporal search by scanning the APD gate, covering as much as 2 μs per second.

- Once acquired, the position of the return within the gate may be determined, and the gate position adjusted to always hold the return at approximately the same place within the gate.

  This helps ensure that the APD response is uniform, and also results in smaller elapsed times for the TDC (if positioning near end of gate). I don't know if the latter is an important concern, but I could see how it might be.

- Auto-guiding is, of course, possible via our control computer. Focus assessment, beam divergence control are also possible.

- The multiple counters allow redundant timing checks. Even if we don't use the CPS counter, the combination of the PPS and free-running ~~clocks~~ counters gives us closure & verification of how many pulses are counted per second.

  Incidentally, one needs 28 bits to count 2.5 seconds' worth of 100 MHz pulses.